NMIX/T-0332

68332 Single Board Computer

Covers: NMIX/T-0332 V1.0 10/13/95

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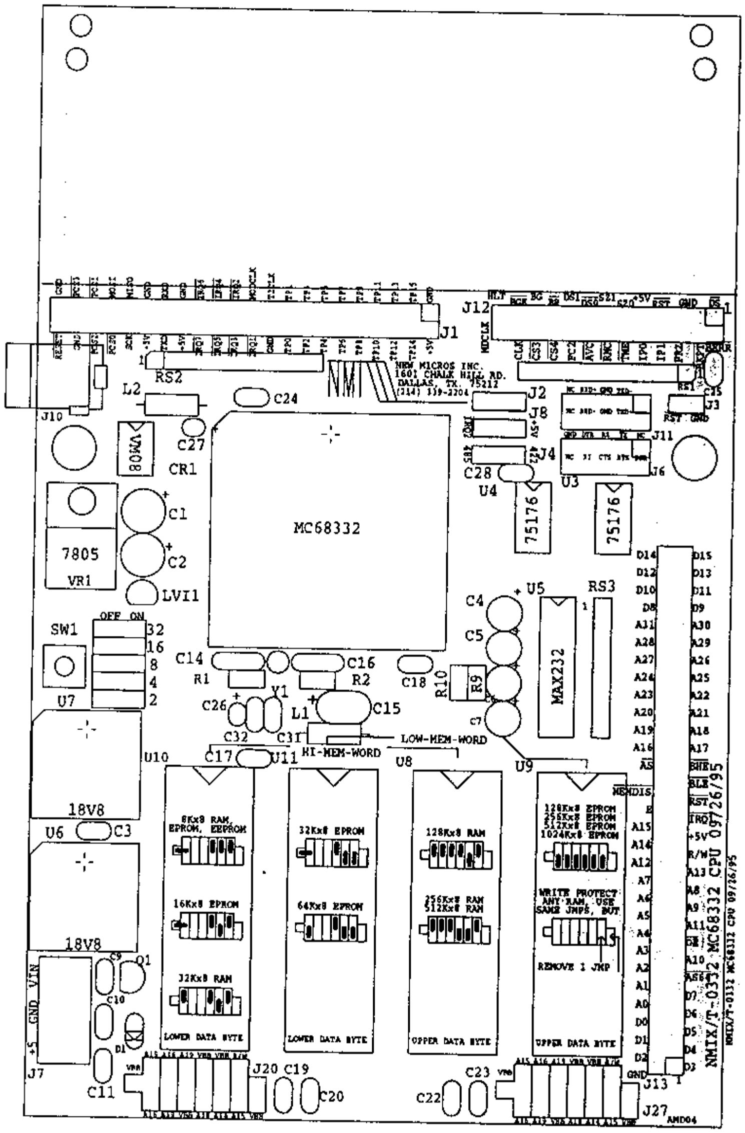
SHORT INTRODUCTION

The NMIX-0332, is an MC68332 based single board computer. When purchased in the NMIX development configuration, it is complete and ready to run. The support circuitry required is held to an absolute minimum through the use of PLDs. A rectifier/regulator section converts 7-18V A.C. (or D.C.) power from an optional wall transformer to usable 5VDC. Screw terminals are provided to accept an external 5VDC supply if preferred. This computer is also available in the NMIT OEM configuration.

The processor has a 16M maximum, address space. Four memory sockets are available for use in this memory space. Decode logic allows various combinations of parts. From 8K, 16K, 32K, 64K, 128K, 256K and 512K, even 1024K devices can be accommodated by jumper settings.

Normally, a developer will use the NMIX-0332 for development, and high end projects, then switch to the lower cost NMIT-0332 (or a modified version of it) when volume buying begins. The NMIT-0332 is a target version of the NMIX-0332. It is made from the same printed circuit board as the NMIX-0332, but has fewer parts installed.



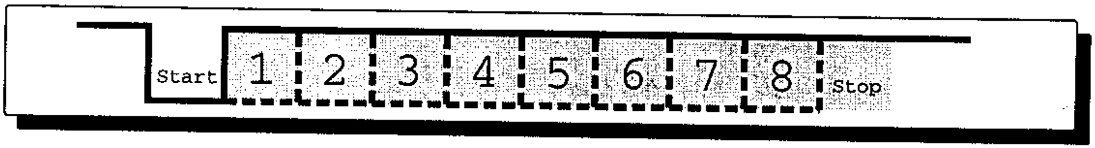
The NMIT-0332, when purchased in the generic target configuration, is a minimum, 5 Volt only, configuration with the MC68332, crystal, reset circuit, PLDs and four 32 pin JEDEC sockets. Typically, a program developed in the "development configured" board will be installed in the "generic target configured" board for production. The user must install the appropriate jumpers, which are not provided in the target configuration. All configurations of the MC68332 based NMIX-0332 boards use the same base PC board. Configuration differences refer to the extent to which the board is filled with components. Custom versions, varying between the fully populated NMIX, and the minimally populated NMIT boards are available from NMI. Call for current pricing and availability.

GETTING STARTED IN Max-FORTH

To operate the NMIX-0332 system, plug in the wall transformer and connect a terminal to the serial RS-232 DB9F connector. Use the DB9 to DB25 adapter if your terminal requires a DB25 termination. Most terminals should plug in directly, with a straight through cable (i.e.: pin 1 to pin 1, 2 to 2, 3 to 3, etc.). The NMIX-0332 uses lines 2 and 3 for serial in and serial out respectively, and pin 7 for ground (pin 5 is electrical ground for the DB9 connector). Many terminals require additional hand shaking signals to work, so pins 4 and 5 are hooked together on the DB25F connector (pins 7 and 8 on the DB9 connector), as are pins 6 and 20 (pins 4 and 6 on the DB9 connector). In this way, terminals that require the additional handshake signals have their own " clear to send" / "ready to send" and "data terminal ready" / "data set ready" signals wrapped back around, indicating "always ready". The table below details the interconnection of pins between J6, a DB9, and a DB25 termination.

J6	DB9F	DB25F	Signal Name
9		1	Case Ground
3	2	2	Serial in
5	3	3	Serial out
9	5	7	Logic Ground
	7 to 8	4 to 5	CTS to RTS
	4 to 6	6 to 20	DSR to DTR

In order to talk to the NMIX-0332 the terminal must have the correct bit settings. The baud rate should be set at 9600 baud. The NMIX-0332 sends and receives a bit protocol of one start bit, eight data bits and one stop bit.



When the tterminal is set correctly, every time you depress and release the reset button the NMIX-0332 should respond with:

```
Max-FORTH Vx.x
```

Seeing that message means the terminal can see the NMIX-0332. Press "return" on your terminal several times. If the NMIX-0332 responds with "OK" each time, communications are established.

Now, you will want to see the system do something. Type WORDS followed by a return. This will cause the system to list its entire vocabulary, some 300 plus words. The listing can be stopped at any time by pressing a key, like the space bar.

Now try a simple program to exercise some of these words. Enter:

```
: TYPE-LETTERS 5B 41 DO I EMIT LOOP ;
TYPE-LETTERS
```

to which the machine will respond:

```
: TYPE-LETTERS 5B 41 DO I EMIT LOOP ; OK
TYPE-LETTERS ABCDEFGHIJKLMNOPQRSTUVWXYZOK
```

Now have a look at memory with the DUMP command. Type:

```
0000 80 DUMP
```

and examine the results (remember we put the machine in HEX).

Enter "WORDS" on the keyboard again and observe that the first word displayed has become the word TYPE-LETTERS defined above.

Max-FORTH IN A NUTSHELL

Max-FORTH closely follows the basic human methodology for dealing with language. Learning a "human" language starts with understanding a few simple word. (I.e.: YES, NO, STOP, GO, etc.). Next, phrases are made from those words. The meanings of phrases are named, and new words are born. Then, larger, more complex concepts are built from these simple beginnings. Complicated words are defined in terms of simpler words. Using the basics, larger and larger concepts are built as vocabulary grows. (E.g. from the few words given above, STOP GO STOP means JERK.)

Suggesting the closeness of this linkage, the program segments in Max-FORTH are called words and are kept in a structure, called the dictionary. The dictionary is a linked list with all known words in the language. Max-FORTH provides a starter set of over 300 words. These are the basics, just enough to begin describing a programming task comfortably. Each word has a very precise meaning, not at all ambiguous. To learn Max-FORTH, a few of these words must be understood. From these simple words, low level phrases can be described. The phrases are given names. Newly defined words can be used in more complex definitions by their name. As the programming task progresses, the number of known words grows. While the later words can be more complex, they are generally easier to understand in terms of named purpose, more like the natural language equivalent.

The last word added to the dictionary fully describes the program to be run. It does so in terms of words already known, which are further described by other, underlying words, etc. The pyramiding structure of lower words can be followed backwards until segments "understandable" by the CPU (i.e.: machine code) are reached. Those machine-coded words were provided in the basic word set already defined in Max-FORTH (The process of descending, from compiled word-pointer, to the next compiled word-pointer, until finding machine code, is called threading.)

A Max-FORTH programmer describes the programming problem by adding new definitions (or words, for short) to the dictionary. They are defined in terms of the words already built into the language, which the machine knows how to translate. The new words are added to the linked list. They become part of the language, describing the problem in terms the computer "understands". As words are added, the dictionary grows. Each added word describes another part of the program more succinctly. A word in Max-FORTH can be evoked by stating its name interactively. When the program is finished the whole program has one name. The program can be invoked by entering its name.

To facilitate dedicated applications, a word can also be started when the computer is reset. An autostarted word has a special demarcation, a recognition pattern and a pointer left in memory, which indicates to the Operating System it should be run. Max-FORTH itself is autostarted in this manner, by the Operating System, if no other autostarted word is found.

Most programs for dedicated applications, are endless loops. The endless loop of the Max-FORTH development language is called the Outer Interpreter. This structure initializes the system, then, repeatedly accepts an input line, translates it, returns for another line, etc.

The syntax of Max-FORTH is remarkable simple. The language is practically free form. The syntax is simply stated: Everything input to the Outer Interpreter is either a word or a number. If the input is not a known word or translatable as a number, it is an error. (The strings found meaningless are echoed back, followed by a question-mark.) Words and numbers are delimited by spaces.

It would be easy to be misled to believe there is more syntax associated with the Outer Interpreter. There is not. Words sometimes have actions in themselves which gives the appearance of syntax. For instance, comments appear to have a syntax. They start with a "(" and end with a ")". A casual reader of Max-FORTH code will be happily able to read most listings, by knowing the things between free standing "(" and ")"s are comments. It is not an action of the language that renders them as an uninterpreted string, but rather the action of the word "(" which throws away the input stream until its matching ")" is found. Thus, the Outer Interpreter only sees the "(", executes it and continues on. The rest of the comment is bypassed as surely as if it were never there.

The feel of syntax, then, comes not from the language interpreter itself, but from the individual words as they are translated. Knowing the specific action of the words is important, then. The most important are the defining words that allow compilation of new definitions. Using the provided words correctly will allow the language to be extended. Words that extend the language are called defining words.

Max-FORTH is both an interpreter and a compiler. This is facilitated by the Outer Interpreter's two states: Interpretation Mode and Compilation Mode. Instructions can be entered to be run "on the fly". This immediate "translation and execution" is done in the Interpretation Mode. In the Compilation Mode, the Outer Interpreter "translates", but, generally, does not "execute" the functions found. If the word has no markings as a word to be executed immediately, the Outer Interpreter defers execution by storing them as executable tokens in memory.

The word that switches the Outer Interpreter from Interpretation Mode to Compilation Mode is ":" (pronounced "colon"). The word that switches it out of Compilation Mode is ";" (pronounced semicolon). When a ":" is interpreted in the input stream, its execution has several effects. The Outer Interpreter is switched to Compilation Mode. Also, the input stream is searched for a string for use as a name for a new definition. This string is used to create a dictionary entry for the new word.

This dictionary entry is called a "head". Linkages are added to the head to allow it to be found in memory. This head will be used for comparison with the input stream by the Outer Interpreter to tell if the new definition is being referenced in the input stream. After changing the Outer Interpreter's state, making the head, and doing some minor error checking, ":" starts the code section of the new word by laying in a pointer to a routine that can translate the two byte tokens. It then returns control back to the Outer Interpreter. The input stream pointer is moved past the string. The Outer Interpreter continues to evaluate the input stream.

Words now found will not be immediately executed. They are compiled as tokens into the code section, or "body", of the new definition being formed. Most functions compile into one 16-bit memory "word" (two bytes). This means compiled Max-FORTH code is very compact. A pointer to the "code" of the word to be later executed is compiled into the next available two-byte spot in the dictionary. This pointer is called the compiled words Code-Field Address. This is a lower level linkage than the dictionary structure, which points to names. Here, the function is referenced by a physical memory address.

This compilation process continues until the word ";" is encountered. The word ";" is from a special class of words which has a precedence flag set, telling the Outer Interpreter not to defer execution, but to run the word whenever found. This allows ";" to run, turning off the Compilation Mode, finishing up the definition, doing some error checking, and enabling the new definition to be found as a new word in the language.

Functions set between a ":" and a "name-string" on the starting end, with a ";" at the end, are compiled into new definitions. After the word has been created, its function can be invoked by including its "name-string" in the input stream with the Outer Interpreter in Compilation Mode. If the outer Interpreter is in Compilation Mode, i.e.: making a newer word, including a word's name in the input stream will cause the previously defined function to be added to a newer words definition. So begins the pyramiding of words upon words until a whole program is described by one word which references all other word definitions required.

For more information on the Max-FORTH language, refer to the Max-FORTH User's Manual, order number UM-MAX.

I/O PORTS

The signal lines for the MC68332's ports are brought out on the 44 pins of J1. The 26 pins of J12 provide access to control signals.

```
                              INPUT/OUTPUT JACK J1
                                     TOP VIEW
   FRONT (EDGE) OF CARD v
                             -     GND  o o +5
                             | X   TP15 o o TP14   X
                             | X   TP13 o o TP12   X
                             | X   TP11 o o TP10   X
                             | X   TP09 o o TP08   X
                             | X   TP07 o o TP06   X
                             | X   TP05 o o TP04   X
        44 pin header        | X   TP03 o o TP02   X
        group                | X   TP01 o o TP00   X
                             | I  T2CLK o o GND
                             | X  MODCK o o /IRQ1  X
                             | X  /IRQ2 o o /IRQ3  X
                             | X  /IRQ4 o o /IRQ5  X
                             | X  /IRQ6 o o /IRQ7  X
                             |      GND o o +5
                             | I    RXD o o TXD    X
                             |      GND o o +5
                             | X   MISO o o SCK    X
                             | X   MOSI o o /PCS0  X
                             | X  /PCS1 o o /PCS2  X
                             | X  /PCS3 o o GND
                             -     GND  o o /RST   I

                         I=INPUT O=OUTPUT X=EITHER
```

These terminations can be used as individual inputs or outputs or in combination. There are very few applications, however, where pins are switched dynamically, sometimes used as inputs,

INPUT/OUTPUT JACK J12

```
                                     TOP VIEW
FRONT (EDGE) OF CARD v
                     -   DS     o o  /BERR
                     |   GND    o o  BKPT
                     |   GND    o o  FRZ
                     |   RST    o o  IP1
                     |   +5V    o o  IP0
                     |   SZ0    o o  /TME
                     |   SZ1    o o  /RMC
     26 pin header   |  /DS0    o o  /AVC
     group           |  /DS1    o o  FC2
                     |  /BR     o o  /CS4
                     |  /BG     o o  /CS3
                     |  /BGK    o o  CLK
                     |  /HALT   o o  MDCLK
```

ASYNCHRONOUS SERIAL I/O

The 68332 has a full duplex hardware serial channel that operates at HC levels. To use this serial channel with standard communications interfaces, level converters are needed. Provisions for RS-232 and RS-422/485 drivers are made on the NMIX/T-0332 boards. A MAX232 IC is used to convert the HC levels to the +/- 3 to +/-15 volts required by the RS-232 specification. J6 is the RS-232 I/O connection. J11 is the RS-422/485 I/O connection. You can use either one or the other by setting the selection jumper on J2. When the leftmost two pins of J2 are connected, RS-232 operation will be enabled. For RS-422/485 operation, remove the MAX232, insert two 75176s (U3 and U4), and move the jumper on J2 to connect the two rightmost pins. Jumper J4 selects between RS-422 and RS-485 operation. RS-422 operation is selected by connecting the two rightmost pins of J4 together.

RS-232 specifies voltage levels referenced to ground. The RS-422 standard uses a voltage differential on a pair of conductors. At full voltage drive levels (+/- 15v) the RS-232 connection has been known to far exceed its 50 foot specificatin even in electrically noisy environments. But it cannot compete with the reliable 4000 foot range of RS-422 signals. RS-422 drivers require only a single +5 Volt supply and operate over inexpensive twisted wire pairs. A full duplex connection for RS-422 requires two twisted pairs, one for transmit, one for receive. Normally a shielded twisted pair cable is employed with the shield acting as the common return path for the signals.

The RS-485 interface uses the same specifications for its transmitters and receivers. However, it premits the use of a single twisted pair for both incoming and outgoing signals. This is accomplished by having a tri-stated transmitter and a tri-stated receiver tied in parallel to the same twisted pair. Multiple drop point systems are possible under this scheme (up to 64 pairs by specification). In practice the transmitter turns on and takes control of the lines only under software control in such a system. The actual implementation of this control will be determined by the particular protocol being used in the communication network. Usually one master sends and addresses messages to one of multiple slaves and then turns off its master transmitter. The addressed slave, recognizing its address will turn on its transmitter and respond with the requested data.

These two interfaces are accommodated on the NMIX-0332 by the addition of two 8 pin 75176's, with each contain a transmitter/receiver pair. J2 routes the RXD signal to either one fo the 75176s (U3) or the R1O of the MAX232. RS232 operation is enabled by jumpering the leftforst two pins. J8 allows U4 to be enabled either from being tied to +5 volts or being switched by IRQ2. The rightmost two pins are jumpered for normal RS232 operation. J4 selects between RS422 and RS485 operation. For RS232 operation the rightmost two pins are jumpered.

ADDRESS DECODING

The chip selects of the four JEDEC sockets are generated by a 18V8Z (U2) a Logic Device. Address configurations supporting the use of 8k, 16k 32k, 64k, 128k, 256k, and 512k static ram memories are defined by jumper settings on configuration block J20. Configuration block J27 allows the use of 8k, 16, 32k, 64k, 128k, 256k, 512k, and 1024k EPROMS in U9 and U11. Memory socket U9 is the upper data byte (even), and U11 is the lower data byte (odd). The RAM is similarly interleaved with U8 being the upper half and U10 being the lower half. A complete diagram of setting jumpers at J27 and J20 for each of the devices mentioned abouve is given in the section on SOCKET JUMPER SETTINGS.

POWER SUPPLY

The power supply circuit on the NMIX-0332 is designed to allow the board to operate from a simple, low-voltage, AC wall-transformer. It has three major sub circuits, rectification, regulation and DC to DC conversion. Battery backup capabilities are also provided to the 32 pin JEDEC sockets and the 68332 internal RAM, and a power-up power-down reset circuit.

The bridge rectifier converts the AC to DC. The 7805 regulates this rectified incoming voltage to a constant 5 Volts. The upper limit of unregulated DC input to the 7805 is set by the ability of the 7805 to dissipate heat. If a heat sink is added to the 7805, voltages in excess of 20 Volts are possible. Driving the 7805 too hard, however, will cause it to enter thermal overload and "shut down" its output.

The typical current required by the NMIX-0332 with 8K CMOS RAM and the Max-FORTH ROM at 16.78 mHz from 9 VAC is 150 mA. An AC "wallbug" style supply delivering 6 to 10 VAC RMS at more than 200 mA. is adequate to power the board. Terminal, J10, is provided with mounting holes to solder in a standard 'barrel-style' AC power connector used with most wall bug style supplies. With CR1 installed you can use virtually any wallbug style supply (AC or DC and you don't need to be concerned about polarity with the DC supply). The overriding requirement is to have about 8 volts DC input for the 7805 while the system is under full load..

BATTERY BACKUP

The battery backup capability allows data retention in otherwise volatile CMOS RAMs and the processor's own internal RAM through main-board power-downs. A third terminal on the power connector, J7, is marked VIN. This the connection for Voltage Battery Backup.

The VIN terminal on J7 is connected to the VBB supply rail on the board by diode, D1. The VBB supply rail supplies the four 32 pin JEDEC sockets, the 8054HN low voltage indicator in the reset circuit, and the MC68332 processor. If no power is applied to the VIN terminal, the VBB rail is supplied through the intrinsic diode of P channel FET, Q1, to within a diode drop of the supplying 5 volt rail (~4.4 Volts). When the 8054HN low voltage indicator releases the reset line, Q1 is turned on and the VBB comes almost completely up to the 5 volt rail (~4.95 Volts). (This may cause some problem with the Dallas Semiconductor DS1223 bat tery sockets, as they "write protect" their RAMs at 4.75 Volts. Running an elevated 5 Volt supply may be necessary to accommodate these parts. The purpose of this feature is, however, to do away with the need for those devices in final system configurations.)

When the 8054HN low voltage indicator holds the reset line low (when VBB is below 3.8-4.2 Volts), Q1 is turned off and the address decoder is disabled through the same input that is used by MEMDIS. This "access" protects the memories during the power down cycle.

To meet the full letter of the specifications of the parts involved the correct backup voltage on the VBB pin is critical. This supply must be low enough to ensure that after the diode drop of D1, the VBB rail cause the 8054HN to issue a reset (~4.0 Volts), otherwise Q1 will remain on and the whole system will be powered by VBB. It must also be high enough to ensure that after the diode drop of D1, the VBB rail will meet the processors required backup voltage (listed as 4.0 Volts). Therefore, the ideal voltage for the VBB supply is 4.3-4.5 Volts. It should be pointed out, however, the Motorola specification appears to be overly conservative. By empirical test, VBB supplies below 3 Volts appear to be quite adequate. Most CMOS RAMs will retain data down to 2.2 Volts. Accounting for the diode drop under such low currents, the VBB supply may work as low as 2.5 Volts.

The processor battery backup supply enters the chip via the Vdds pin. For backup of the processor's RAM to be successful Vstby is connected to Vddsin on the circuit card. When the VBB supply is used on the processor, it will retain its User Area through power down and remember its linkages to the external FORTH dictionary.

BOARD MOUNTING

The NMIX-0332 has six through holes intended for mounting the card. Each hole is drilled at 0.110 inches, clearance for 4-40 hardware. Use caution when installing to prevent inadvertent grounding of printed circuit board traces. The mounting hole just below J13 is the only that has a trace located nearby. Additional boards may be stacked above or below, as desired, on the female of male side of the Vertical Stacking Connector (VSC).

Common, 3/4 inch long, hex standoffs with a male screw on one end and a female threaded hole on the other are ideal interboard connection devices. The VSC connector was designed to work with this size spacer, giving reliable board to board mounting.

The length of the standard spacer, 0.750 inches, plus the board thickness, 0.061 inches, gives a nominal board to board spacing of 0.811 inches. Should an exact spacing of 0.800 inches be required, as in the case of standard mounting hardware haviong 0.800 inch PCB card guides, The standard spacer will have to mbe milled to reduce its length by 0.011 inches.

TROUBLESHOOTING

As always the first thing to do when troubleshooting is to check the power and ground connections. An oscilloscope should be used to check signals. The heat sink of the 7805 is a con venient place to hook a ground clip. If +5 Volts is present at J7 and the board is not operational, the next item to check is the oscillator. Putting the scope on CLKOUT (Pin 24 J12) should show a high frequency sine wave varying from about .5 Volt lows to 4.5 Volt peaks. If the clock signal is not present check to see if there is +5V present at the power pin Vdd (Pins 1, and 59 on U1). An accessible test point for this check is either end of L2. If the clock signal is not present and Vdd is at +5 volts, then either the MC68332 or the crystal are bad and require replacement. There is one exception. If the processor has executed a STOP instruction, the oscillator will stop. When the oscillator is functioning correctly a clean running square wave should be present at the CLKOUT. The CLKOUT signal drives the timing for all external memory transfers. This signal should transition nearly rail to rail, a 0.4V low and a 4.6V high are normal. Less amplitude can indicate a board short or an excessive load on the line external to the MC68332.

The serial channel should send a sign-on message to the terminal. If not, the reset circuit could be bad, the serial converter (U5) could have failed, or the MC68332 could be defective. With the reset button depressed the RESET line (Pin 44 J1) should be at ground. When release, the pin should rise to 5 Volts in about a quarter second. If the reset pin is working and still no message is seen on the terminal, check TXD, the serial output line, at pin 11 on U5. When reset is exercised, this line should go from normally high through a multitude of toggles back to a high state. The periods of the toggle transitions are multiples of approximately 100 microseconds. If this signal is not present, and there are no user ROMs in the board, the MC68332 is suspect. If the signal is present, check pin 3 of the DB25F connector. It should normally be at -V (-9 Volts nominally) and should toggle to +V (+9 Volts nominally) at the same rate as the serial output line. If this is happening and no message is seen, the RS-232 wiring or the terminal is suspect. Check to see if J6 is connected to the DB25F RS-232 connector as follows:

J6	DB25F	Signal Name
n/c	1	Case ground
5	2	Serial in (to NMIX-0332)
3	3	Serial out (from NMIX-0332)
9	7	Electrical ground

Check the voltages on pins 2 and 3 of the DB25 connector. If pin 3 is very negative and pin 2 is floating, both systems are trying to talk on the same line. Pins 2 and 3 need to be swapped. Usually this is done with a "null modem" inserted where the two systems connect.

If the -V/+V signal was not found at pin 3, the RS-232 converter is not working. Check pin 2 of the MAX232 for +V and pin 6 of the MAX232 for -V. If these signals are not present, the charge pump of the MAX232 has failed. Pin 14 of the MAX232, the output, should look the same as pin 5 of J6.

Check pin 3 of J6 which is the serial into the board from the terminal. It should normally be at a negative voltage between -3 and -15 Volts. When a key is pressed on the terminal it should pulse to positive voltages between +3 and +15 Volts. If it doesn't, the terminal or the RS-232 wiring are suspect. The same signals at inverted TTL levels, should also be at RXD, which is the serial input line of the processor.

The most common error in trying to use the NMIX-0332 is mismatched baud rates or bit set tings. Verify that the terminal is set for 9600 baud with one start bit, eight data bits and one stop bits, with no parity generated. Also, make sure that the terminal software is set up properly.

MEMORY MAP

The MC68332 offers the user an contiguous address space of 1 megabyte which is split into 16-64kbyte banks. On power up, the 1k byte internal ram on the MC68332 maps to $00000 so that it will be avialable to the user even if there is no additional external ram available.

K#	**HEX**

MISCELLANEOUS JUMPERS

#	SOURCE	DESTINATION	NORMALLY
J2			
R1O-J2,2	U5 PIN 12	U1 PIN 17	CLOSED
J2,2-RO	U1 PIN 17	U3 PIN 1	OPEN
J4			
IRQ2-J4,2	U1 PIN 77	U3 PIN 2&3	OPEN (485)
J4,2-GND	U3 PIN 2&3	GROUND	CLOSED(422)
J8			
IRQ2-J8,2	U1 PIN 77	U4 PIN 2&3	OPEN
J8,2-+5V	U4 PIN 2&3	+5 VOLR RAIL	CLOSED

GENERAL PURPOSE SOCKETS

JUMPER	1 ○	○ 32	+5	
A16	2 ○	○ 31	JUMPER	
JUMPER	3 ○	○ 30	JUMPER	VCC
A12	4 ○	○ 29	JUMPER	A14
A7	5 ○	○ 28	JUMPER	A13
A6	6 ○	○ 27	~~A27~~	A8
A5	7 ○	○ 26	A9	
A4	8 ○	○ 25	A11	
A3	9 ○	○ 24	OE	
A2	10 ○	○ 23	A10	
A1	11 ○	○ 22	CHIP SELRCT	
A0	12 ○	○ 21	IO/7	
IO/0	13 ○	○ 20	IO/6	
IO/1	14 ○	○ 19	IO/5	
IO/2	15 ○	○ 18	IO/4	
GND	16 ○	○ 17	IO/3	

	A15	A16	A19	VBB	VBB	R/W	
	○	○	○	○	○	○	
VBB ○	○3	○1	○21	○29	○30	○31	○
	○	○	○	○	○	○	○
	A16	A19	+5	A18	A14	A15	VBB

GENERAL PURPOSE SOCKET - U8, U9, U10, U11

3 31 1 30 28 29

MEMORY JUMPER SETTINGS

```
Jumper Settings for Standard JEDEC 28/32/36  Pin Devices
```

```
8K X 8 DEVICES
2764, 2864, 6264

                 A15   A16   A19   VBB   VBB   R/W
                +-----+-----+-----+-----+-----+-----+
          +-----|     |     |     |  X  |  X  |  X  |-----+
          |  XXXXXXX  |     |     |  X  |  X  |  X  |     |
          +-----|     |     |     |     |     |     |     |
                +-----+-----+-----+-----+-----+-----+-----+
            VBB   A16   A19   VBB   A18   A14   A15   VBB

           (+5     PIN3   PIN1 PIN28 PIN29 PIN30 PIN31)
                      (CENTER PIN DESIGNATION)
```

```
16K X 8 EPROM
27128
                 A15   A16   A19   VBB   VBB   R/W
                +-----+-----+-----+-----+-----+-----+
          +-----|     |     |     |  X  |     |  X  |-----+
          |  XXXXXXX  |     |     |  X  |  X  |  X  |     |
          +-----|     |     |     |     |  X  |     |     |
                +-----+-----+-----+-----+-----+-----+-----+
            VBB   A16   A19   VBB   A18   A14   A15   VBB

           (+5     PIN3   PIN1 PIN28 PIN29 PIN30 PIN31)
                      (CENTER PIN DESIGNATION)
```

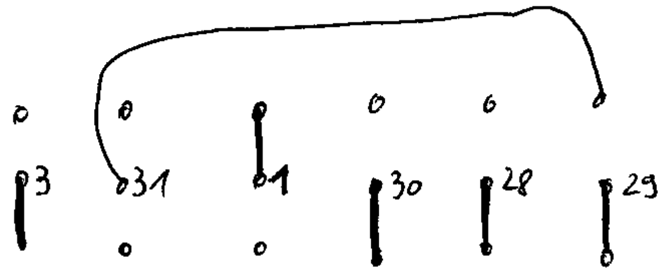
```
32K X 8 EPROM
27256
              A15   A16   A19   VBB   VBB   R/W
            +-----+-----+-----+-----+-----+-----+
      +-----|     |     |     |  X  |     |     |-----+
      |  XXXXXXX  |     |     |  X  |  X  |  X  |     |
      +-----|     |     |     |     |  X  |  X  |     |
            +-----+-----+-----+-----+-----+-----+-----+
       VBB   A16   A19   VBB   A18   A14   A15   VBB

      (+5   PIN3  PIN1 PIN28 PIN29 PIN30 PIN31)
                (CENTER PIN DESIGNATION)
```

```
32K X 8 RAM
62256

              A15   A16   A19   VBB   VBB   R/W
            +-----+-----+-----+-----+-----+-----+
      +-----|  X  |     |     |  X  |     |  X  |-----+
      |     |  X  |     |     |  X  |  X  |  X  |     |
      +-----|     |     |     |     |  X  |     |     |
            +-----+-----+-----+-----+-----+-----+-----+
       VBB   A16   A19   VBB   A18   A14   A15   VBB

      (+5   PIN3  PIN1 PIN28 PIN29 PIN30 PIN31)
                (CENTER PIN DESIGNATION)
```



29F010
0 40

64K X8 EPROM

```
        A15   A16   A19   VBB   VBB   R/W
      +-----+-----+-----+-----+-----+-----+
+-----|     |     |     |  X  |     |     |-----+
|     |  X  |     |     |  X  |  X  |  X  |     |
+-----|  X  |     |     |     |  X  |  X  |     |
      +-----+-----+-----+-----+-----+-----+-----+
 VBB   A16   A19   VBB   A18   A14   A15   VBB

 (+5    PIN3  PIN1 PIN28 PIN29 PIN30 PIN31)
          (CENTER PIN DESIGNATION)
```

128K X 8 RAM

```
        A15   A16   A19   VBB   VBB   R/W
      +-----+-----+-----+-----+-----+-----+
+-----|  X  |  X  |  X  |  X  |     |  X  |-----+
|     |  X  |  X  |  X  |  X  |  X  |  X  |     |
+-----|     |     |     |     |  X  |     |     |
      +-----+-----+-----+-----+-----+-----+-----+
 VBB   A16   A19   VBB   A18   A14   A15   VBB

 (+5    PIN3  PIN1 PIN28 PIN29 PIN30 PIN31)
          (CENTER PIN DESIGNATION)
```

256K X 8 RAM/512K X 8 RAM

```
        A15   A16   A19   VBB   VBB   R/W
      +-----+-----+-----+-----+-----+-----+
+-----|  X  |  X  |  X  |     |     |  X  |-----+
|     |  X  |  X  |  X  |  X  |  X  |  X  |     |
+-----|     |     |     |  X  |  X  |     |     |
      +-----+-----+-----+-----+-----+-----+-----+
 VBB   A16   A19   VBB   A18   A14   A15   VBB

 (+5    PIN3  PIN1 PIN28 PIN29 PIN30 PIN31)
          (CENTER PIN DESIGNATION)
```

128K X 8, 256K X 8, 512K X 8, 1024K X 8   EPROM

```
          A15   A16   A19   VBB   VBB   R/W
           +-----+-----+-----+-----+-----+-----+
     +-----|     |     |     |     |     |     |-----+
     |     |  X  |  X  |  X  |  X  |  X  |  X  |     |
     +-----|  X  |  X  |  X  |  X  |  X  |  X  |     |
           +-----+-----+-----+-----+-----+-----+-----+
       VBB   A16   A19   VBB   A18   A14   A15   VBB


     (+5    PIN3  PIN1 PIN28 PIN29 PIN30 PIN31)
                (CENTER PIN DESIGNATION)
```

To write protect the ram use the same addressing scheme jumpers given in the previous examples but add the following pull up resistor.

```
                     REMOVE THIS JUMPER ----+
                                            |
                                            |
                                            |
          A15   A16   A19   VBB   VBB   R/W |
           +-----+-----+-----+-----+-----+--|--+ VBB
     +-----|     |     |     |     |     |  |  |-----+
     |     |  X  |  X  |  X  |  X  |  X  |  X  |     |
     +-----|  X  |  X  |  X  |  X  |  X  |  X  |     |
           +-----+-----+-----+-----+-----+-----+--|--+
       VBB   A16   A19   VBB   A18   A14   A15    |
                                                  |
                                                  |
                                                  |
 ADD A 100K 1/4 4 5% RESISTOR ACROSS THESE PINS---+


     (+5    PIN3  PIN1 PIN28 PIN29 PIN30 PIN31)
                (CENTER PIN DESIGNATION)
```

EXPANSION JACK J13

D14	o o	D15
D12	o o	D13
D10	o o	D11
D8	o o	D9
A31	o o	A30
A28	o o	A29
A27	o o	A26
A24	o o	A25
A23	o o	A22
A20	o o	A21
A19	o o	A18
A16	o o	A17
/AS	o o	/BHE
/MEMDIS	o o	/BLE
E	o o	/RST
A15	o o	/IRQ1
A14	o o	+5
A12	o o	R/W
A7	o o	A13
A6	o o	A8
A5	o o	A9
A4	o o	A11
A3	o o	/OE
A2	o o	A10
A1	o o	/AS6
A0	o o	D7
D0	o o	D6
D1	o o	D5
D2	o o	D4
GND	o o	D3

The J13 expansion connector was designed to follow the JEDEC standard for byte sized memory parts in the 8, 16 and 32K Byte varieties.

SERIAL INPUT/OUTPUT JACK J11 (RS442/485)

```
                  TOP VIEW

(PIN 1)     N.C.  o  o  N.C.
        +422XMT  o  o  -422XMT
            GND  o  o  GND
        -485RCV  o  o  +422RCV
           N.C.  o  o  N.C.
```

SERIAL INPUT/OUTPUT JACK J6 (RS232)

```
                 TOP VIEW

(PIN 1)    N.C.    o  o  TO J6-7 (DSR)
           RX      o  o  TO J6-6 (RTS)
           TX      o  o  TO J6-4 (CTS)
  (DTR) TO J6-2    o  o  N.C.
           GND     o  o  N.C.
```

FACTORY DEFAULT SETTING FOR RS232

```
+---+---+---+
| XXXXX | o |      J2
+---+---+---+

+---+---+---+
| o | XXXXX |      J8
+---+---+---+

+---+---+---+
| o | XXXXX |      J4
+---+---+---+
```

PROGRAMMING EXAMPLES

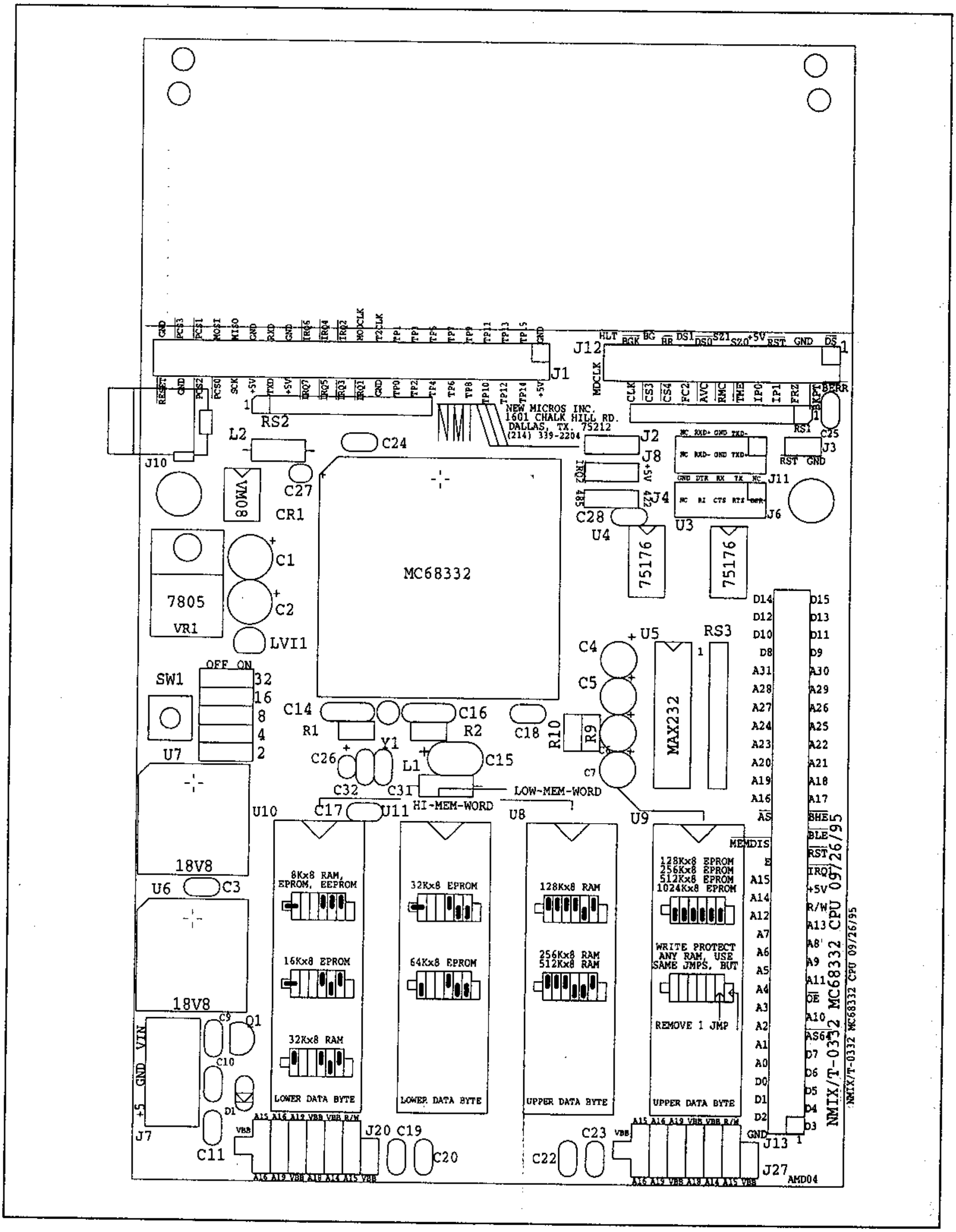
NMIX-0332 PARTS LIST

REF.DES.	VALUE	COMPONENT
C1-3,8-10,14-22	0.1uF 50v	Ceramic
C24,26,27		
C4-7	10uF 16v	Electrolytic
C11,12	22pF 10v	Disk Ceramic
C13	0.1uF 25V	Mylar low leakage
C25	1.0mF 16v	Electrolytic
C29	100uF 16v	Electrolytic
R1	15k,1/4w,5%	Resistor
R2	10meg,1/4w,5%	Resistor
R3-6	10k,1/4w,5%	Resistor
RS1,RS2	10K sip,5%	Common and 9 resistors
RS3	10k sip,5%	Common and 7 resistors
U1	MC68332	Microcontroller
U2 (not used)		
U3,4	75176	IC
U5	MAX232	IC
U6,7	18V8Z	PAL
*U8,10	HM658512ALP-10	512K X 8 SRAM
*U9	27C256	HI BYTE ROM
*U11	27C256	LO BYTE ROM
LVI1	8054	IC
*VR1	LM7805	REGULATOR
*CR1	VM08	BRIDGE RECTIFIER
D1	1N4148	SILICON DIODE
Q1	VP0300M	FET
L1,2	10uH	INDUCTOR
SW1		RESET SWITCH
	132 PIN PLCC	SOCKET U1
	8 PIN DIP	SOCKET U3, U4
	16 PIN DIP	SOCKET U5
	20 PIN PLCC	SOCKET U6,U7
	32 PIN DIP	SOCKET U8,9,10,11
*J20,27	2 PIN	SOCKET
	1X6 2EA	HEADER
	1X7 1EA	HEADER
*J10	POWER JACK	CONNECTOR
Y1	32.768kHz	XTAL
*J13	VS 60 PIN	CONNECTOR
	VS 34 PIN	SPACER
*J7	3 PIN	TERMINAL BLOCK

J6,11	2X5 DBL PIN	HEADER
J2,4,8	1X3 PIN	HEADER
J14	3X5 PIN	HEADER
	NMIX-0332	PCB
	SHUNTS	

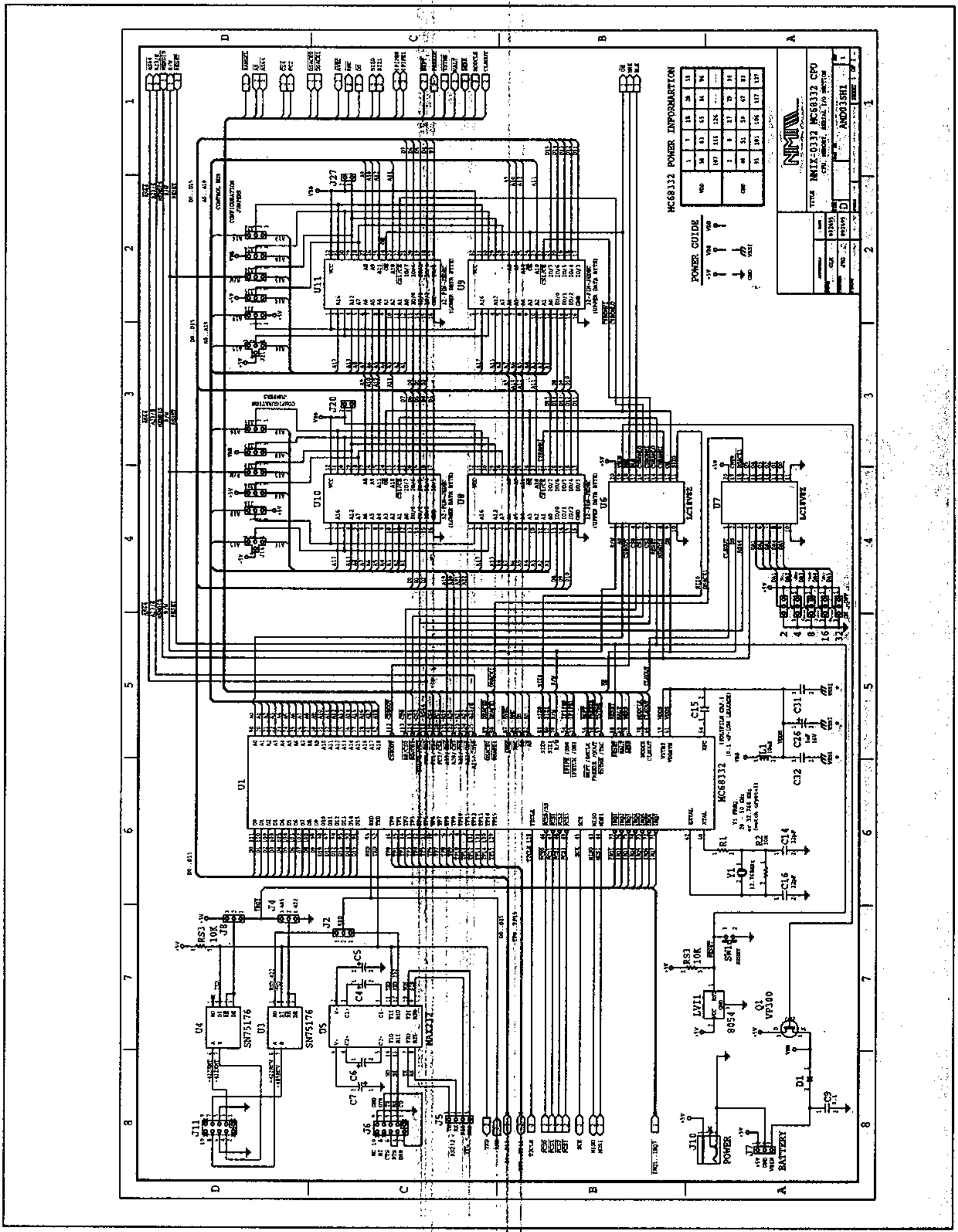
Items marked with and '*' are inluded with the NMIX-0332 only.

SILKSCREEN

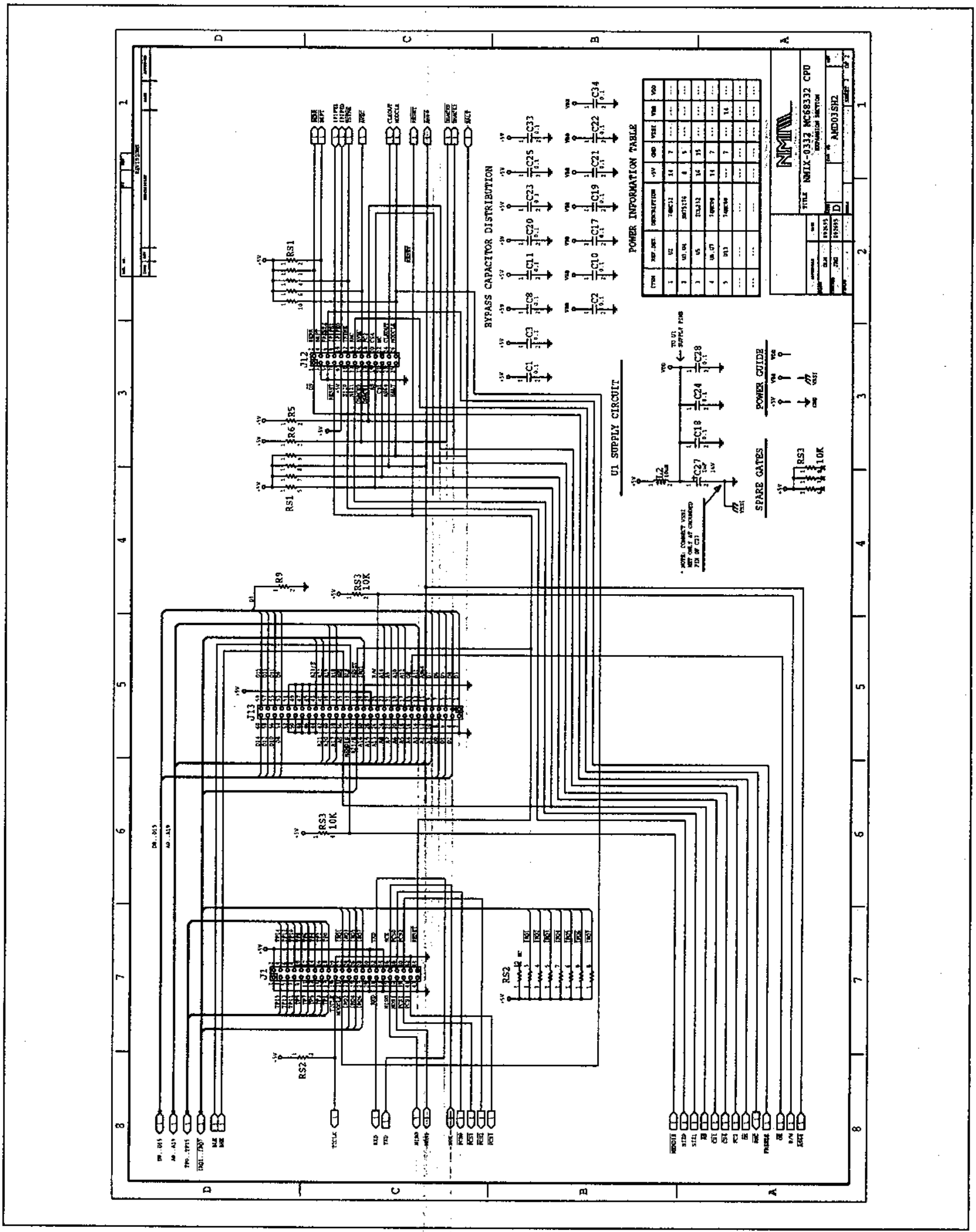


J1
GND
PCS3
PCS1
MOSI
MISO
GND
RXD
GND
IRQ6
IRQ4
IRQ2
MODCLK
T2CLK
TP1
TP3
TP5
TP7
TP9
TP11
TP13
TP15
GND
RESET
GND
PCS2
PCS0
SCK
+5V
TXD
+5V
IRQ7
IRQ5
IRQ3
IRQ1
GND
TP0
TP2
TP4
TP6
TP8
TP10
TP12
TP14
+5V
J12
HLT
BGK
BG
BR
DS1
DS0
SZ1
SZ0
+5V
RST
GND
DS
1
MDCLK
CLK
CS3
CS4
FC2
AVC
RMC
TME
IP0
IP1
FRZ
BKPT
BERR
RS1
C25
1
RS2
L2
C24
J10
NM
NEW MICROS INC.
1601 CHALK HILL RD.
DALLAS, TX. 75212
(214) 339-2204
J2
J8
IRQ2
+5V
485
422
J4
C28
NC RXD+ GND TXD-
NC RXD- GND TXD+
GND DTR RX TX NC
NC RI CTS RTS DSR
J11
J6
J3
RST GND
U3
U4
75176
75176
VM08
C27
CR1
MC68332
7805
VR1
C1
C2
LVI1
SW1
OFF ON
32
16
8
4
2
U7
C14
C16
R1
R2
C18
R10
R9
Y1
C26
L1
C15
C4
C5
C6
C7
+ U5
RS3
1
MAX232
C32
C31
LOW-MEM-WORD
HI-MEM-WORD
C17
U11
U10
U8
U9
18V8
U6
C3
18V8
8Kx8 RAM,
EPROM, EEPROM
16Kx8 EPROM
32Kx8 RAM
LOWER DATA BYTE
32Kx8 EPROM
64Kx8 EPROM
LOWER DATA BYTE
128Kx8 RAM
256Kx8 RAM
512Kx8 RAM
UPPER DATA BYTE
MEMDIS
128Kx8 EPROM
256Kx8 EPROM
512Kx8 EPROM
1024Kx8 EPROM
WRITE PROTECT
ANY RAM, USE
SAME JMPS, BUT
REMOVE 1 JMP
UPPER DATA BYTE
D14
D12
D10
D8
A31
A28
A27
A24
A23
A20
A19
A16
AS
E
A15
A14
A12
A7
A6
A5
A4
A3
A2
A1
A0
D0
D1
D2
GND
D15
D13
D11
D9
A30
A29
A26
A25
A22
A21
A18
A17
BHE
BLE
RST
IRQ1
+5V
R/W
A13
A8
A9
A11
OE
A10
AS64
D7
D6
D5
D4
D3
J13
1
NMIX/T-0332 MC68332 CPU 09/26/95
NMIX/T-0332 MC68332 CPU 09/26/95
VIN
GND
+5
J7
C9
Q1
C10
D1
C11
A15 A16 A19 VBB VBB R/W
VBB
A16 A19 VBB A18 A14 A15 VBB
J20
C19
C20
C22
C23
A15 A16 A19 VBB VBB R/W
VBB
A16 A19 VBB A18 A14 A15 VBB
J27
AMD04

SCHEMATIC 1 OF 2



SCHEMATIC 2 of 2


BYPASS CAPACITOR DISTRIBUTION
POWER INFORMATION TABLE
U1 SUPPLY CIRCUIT
POWER GUIDE
SPARE GATES
TO U1 SUPPLY PINS
J12
J13
J1
RS1
RS2
RS3 10K
R5
R6
R9
C1
C2
C3
C8
C10
C11
C17
C18
C19
C20
C21
C22
C23
C24
C25
C27
C28
C33
C34
L2
NMIX-0332 MC68332 CPU
EXPANSION SECTION
AMD03SH2
D
A
B
C
1
2
3
4
5
6
7
8